CLAIMS

Following are a set of clean, rewritten Claims in accordance with amendments made herein.

1. (Twice Amended) A delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising:

an inverter chain containing not less than one inverter; and

a metal-oxide-semiconductor capacitor, known as a MOS capacitor, having a single transistor per stage of the inverter chain connected to an output section of the inverter and, when a logic signal having a targeted logic level is input, changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter, wherein each stage is tied alternately to one of a power voltage source and a ground voltage source, said MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage.

2. (Twice Amended) A delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprises:

an inverter chain containing not less than one inverter; and

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a metal-oxide-semiconductor capacitor, known as a MOS capacitor, having a single transistor per stage of the inverter chain connected to an output section of the inverter and exhibiting changes in its capacitance to correspond with changes in output resistance of the inverter in relation to a source voltage, wherein each stage is tied alternately to one of a power voltage source and a ground voltage source, said MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage.

15. (Amended) A delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprises:

an inverter chain containing not less than four inverters;

a p-channel metal-oxide-semiconductor transistor and an n-channel metal-oxide-semiconductor transistor, known as MOS transistors, to comprise each of the at least four inverters, wherein a gate threshold voltage of each gate is shifted in mutually opposing directions;

low threshold voltage n-MOS transistors of each of a first and a third inverter connected to ground by a high threshold voltage n-MOS transistor; and

low threshold voltage p-MOS transistors of each of a second and a fourth inverter connected to ground by a high threshold voltage p-MOS transistor;

wherein, when an input logic signal is fixed at a low level during a standby state, said high threshold voltage n-MOS transistor is set to an off-state in response to a chip select signal controlling said standby state, and said high threshold voltage p-MOS transistor is set to an off-state in response to said chip select signal that is negated.

16. (Amended) A method for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising the steps of:

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(a) setting a metal-oxide-semiconductor capacitor disposed on a transmission path of a logic signal to an off-state in an initial stage; and

(b) changing the metal-oxide-semiconductor capacitor to an on-state from the off-state according to a logic level of the logic signal, said metal-oxide-semiconductor capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage.

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18. (Amended) A delay circuit comprising a plurality of cascading gate circuits and a plurality of MOS capacitors connected to the output sections of said gate circuits, wherein: all the MOS capacitors are connected so as to turn from the off-state to the on-state when the logic signal having the logic level targeted for delay is input into the head gate circuit among said cascading gate circuits, each of said MOS capacitors represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage.